(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 April 2002 (11.04.2002)

PCT

(10) International Publication Number
WO 02/29950 A2

(51) International Patent Classification[7]: H02H

(21) International Application Number: PCT/US01/42574

(22) International Filing Date: 6 October 2001 (06.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/684,350 6 October 2000 (06.10.2000) US

(71) Applicant: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121-1724 (US).

(72) Inventor: APARIN, Vladimir; 4126 Calle Mar De Ballenas, San Diego, CA 92130 (US).

(74) Agents: WADSWORTH, Philip, R. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

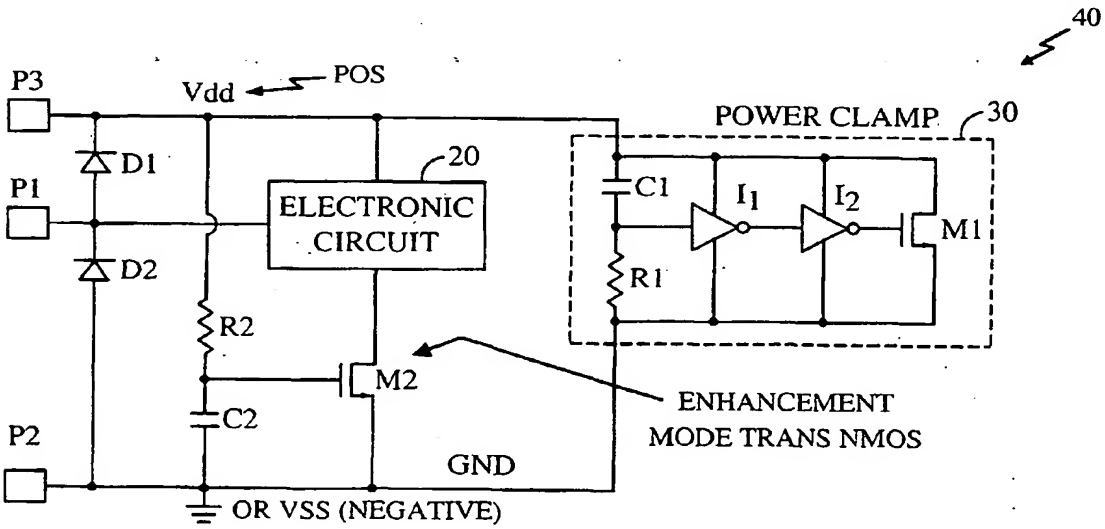
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT



(57) Abstract: An arrangement for protecting an element from electro-static discharge. A switch is provided to inhibit the flow of energy through the element in response to the control signal. In the illustrative embodiment, the switch is a transistor switch. A resistor is disposed between an input terminal of the transistor and the positive supply to keep the transistor on during normal operation. A capacitor is disposed between the input terminal of the transistor and ground to prevent the input voltage of the transistor from fast changing. The RC time constant is chosen to be much larger than the time constant of the ESD pulse. Consequently, input voltage of the transistor will remain unchanged near ØV and the transistor will remain off during ESD event preventing the element from conducting the discharge current and providing ESD protection.

WO 02/29950 A2

ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to electrical and electronic circuits and systems. More specifically, the present invention relates to systems and methods for protecting electrical and electronic circuits and systems from electro-static discharge.

Description of the Related Art:

Many electronic circuits and systems are susceptible to being damaged by electro-static discharges. An electro-static discharge is a charge transfer from a charged body, often a human, to ground or a terminal of opposite polarity. Electro-static discharges can generate energy with tens of thousands of volts. When voltages at this level are applied to unprotected and relatively delicate integrated circuits, damage often results. Not only can the operation of the device be momentarily impaired (with the consequent impairment of the operation of the host system and the data output thereby), but, it may also lead to permanent damage. In some cases, the damage to the circuits may be difficult to detect. In any event, it is therefore common in the art to provide some means and methodology for protecting components, circuits, and systems from electrostatic discharge.

One currently used technique for providing protection against electro-static discharge (ESD) is based on the use of a protection circuit consisting of two diodes connected between the device input, supply and ground to shunt positive and negative discharge voltages to supply and/or ground. Unfortunately, the conventional diode based ESD circuit has been found to be less than fully effective in that during an ESD event, until the diodes turn on, some current flows through the protected device or circuit instead of being shunted away by the diodes. If the device is not properly sized

with respect to current handling ability, it may be permanently damaged by the event as discussed above.

Another approach has involved the use of a resistor in front of the device being protected. However, for circuits operating at radio frequencies (RF), resistors used for ESD protection adversely impact performance.

Hence, a need remains in the art for an improved electro-static discharge protection system or method, particularly for use with RF device, circuits and systems.

SUMMARY OF THE INVENTION

The need in the art is addressed by the system and method of the present invention. The inventive system includes an arrangement for protecting an element from electro-static discharge and includes a mechanism for sensing a pulse of energy associated with an electro-static discharge and providing a control signal in response thereto. A switch is provided which inhibits the flow of energy through the element in response to the control signal.

In the illustrative embodiment, the switch is an n-channel field effect (NFET) transistor switch. The switch may be disposed between the element and ground, between the element and source of supply current, and in the input line of the element. In the first case, a resistor is disposed between the positive supply of the element and an input terminal of the transistor to provide a control voltage effective to keep the transistor on during normal operation. A capacitor is disposed between the input terminal of the transistor and ground. The RC time constant is chosen to be much larger than the time constant of the ESD pulse. Consequently, input voltage of the transistor will remain unchanged and the transistor will remain off preventing the element from conducting the pulse discharge current and providing ESD protection.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of an arrangement for providing ESD protection implemented in accordance with conventional teachings.

Fig. 2(a) is a diagram showing the current flow through the port P1, the first diode D1, the positive supply line V_{dd}, the clamp device M1 and GND as a function of time during an ESD event according to a human body model.

Fig. 2(b) is a diagram showing the gate voltage of the clamping transistor M1 as a function of time during the ESD event represented in Fig. 2(a).

Fig. 2(c) is a diagram showing the input current of the electronic circuit with the conventional arrangement and with the arrangement of the present invention.

Fig. 2(d) is a graph illustrating a desired decay time of a network relative to the time constant of the ESD event in accordance with the Human Body Model.

Fig. 3 is a schematic diagram of an illustrative arrangement for providing ESD protection in accordance with the teachings of the present invention.

Fig. 4 is a first alternative embodiment of an illustrative implementation of the ESD protection arrangement constructed in accordance with the present teachings.

Fig. 5 is a second alternative embodiment of an illustrative implementation of the ESD protection arrangement constructed in accordance with the present teachings.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a schematic diagram of an arrangement for providing ESD protection implemented in accordance with conventional teachings. The arrangement 10 is intended to protect an electronic circuit 20 disposed between a source of supply voltage V_{dd} and ground (GND). The circuit 20 has an input terminal P1. As shown in Fig. 1, the conventional arrangement 10 includes first and second diodes D1 and D2 connected in series between the source of supply voltage V_{dd} and ground. The anode of the first diode D1 is connected to the input terminal P1 of the electronic circuit 20. The cathode of the second diode D2 is connected to the input terminal P1. The anode of the second diode D2 is connected to ground at a second terminal P2. The cathode of the first diode D1 is connected to the source of supply voltage V_{dd} at a third terminal P3.

A conventional power clamp 30 is connected between P3 and P2. The clamp 30 includes an n-channel metal-oxide semiconductor transistor M1 biased by an RC network including a first capacitor C_1 connected in series with a first resistor R_1 between V_{dd} and GND. The junction between R_1 and C_1 is connected to the gate of M1 through a buffer amplifier arrangement including first and second series connected inverters I_1 and I_2. The power clamp 30 ensures a low impedance path from the positive supply V_{dd} to the negative supply (GND) during a positive polarity ESD pulse applied to the input pin P1.

When a positive ESD pulse is applied between the signal pin P1 and the ground pin P2. The first diode D1 turns on forcing the positive supply voltage V_{dd} to rise with the ESD pulse. The rising V_{dd} is coupled through C_1 to the input of the first inverter (I_1) forcing its output low. In response, the output of the second inverter (I_2) goes high turning on M1. When M1 turns on, the ESD discharge current starts flowing along the path:

$$P1 \rightarrow D1 \rightarrow V_{dd} \rightarrow M_1 \rightarrow P2(GND)$$

Unfortunately, M1 turns on with a delay equal to the sum of the delays through I_1 and I_2. This is depicted in Fig. 2.

Fig. 2(a) is a diagram showing the current flow through P1, the first diode D1, V_{dd}, M1 and GND as a function of time during an ESD event according to a human body model.

Fig. 2(b) is a diagram showing the gate voltage of the clamping transistor M1 as a function of time during the ESD event represented in Fig. 2(a).

Fig. 2(c) is a diagram showing the input current of the electronic circuit 20 with the conventional arrangement 10 and with the arrangement of the present invention. As shown in Figs. 2(a), (b) and particularly (c), during the delay in the activation of M1, some of the ESD discharge current may flow through the electronic circuit to GND potentially damaging the electronic circuit 20. This undesirable current flow through the electronic circuit is possible if the latter presents a lower impedance path then that provided by the ESD diode D1 and the clamp M1 during the M1 turn-on delay. The arrangement of the present invention is designed to prevent the flow of current through the electronic circuit depicted in Fig. 2(c).

Fig. 3 is a schematic diagram of an illustrative arrangement for providing ESD protection in accordance with the teachings of the present invention. The supply clamp arrangement 40 of the present invention is similar to the conventional arrangement 10 with the exception that a switch M2 is disposed in the ground path of the electronic circuit 20. In the best mode, the switch is an enhancement mode n-channel metal-oxide

semiconductor field-effect transistor (MOSFET). The gate of M2 is coupled to the positive supply V_{dd} through a second resistor R_2.

During normal operation, M2 is on providing the closed ground path for the circuit. The gate of M2 is also coupled to its source through a second capacitor C_2. The ESD event usually occurs when the electronic circuit is unbiased. In this unbiased condition, all voltages in the circuit are the same. So, the gate-source voltage of M2 is zero volts or close to zero volts and M2 is off. During the ESD event, capacitor C_1 starts charging through R_2. If the time constant τ_2 of R_2C_2 is much (e.g., approximately an order of magnitude) larger than the decay time τ_{esd} of the ESD pulse, then the gate-source voltage of M2 should not shift significantly during the ESD event and M2 will stay off. This is illustrated more clearly below with reference to Fig. 2(d).

Fig. 2(d) is a graph illustrating a desired decay time of the network relative to the time constant of the ESD event in accordance with the Human Body Model. As shown in Fig. 2(d), the time constant of the R_2C_2 network, $\tau 2$, should satisfy the condition:

$$\tau_2 = R_2C_2 \geq 10\tau_{esd} \qquad [1]$$

For the Human Body Model (HBM), the ESD event is modeled by a 100pF capacitor charged to some high voltage of several kV and commutated to the circuit input through 1.5 kΩ resistor modeling the human body resistance. Accordingly,

$$\tau_{esd} \approx 1.5\ k\Omega \bullet 100\ pF = 0.15\ \mu s \qquad [2]$$

Since, from equations [1] and [2], τ_2 should be greater than or equal to $10\tau_{esd}$, then τ_2 should be greater than or equal to $10 \bullet 0.15\ \mu s$ or $1.5\ \mu s$ for the case of the Human Body Model.

This will prevent any ESD discharge currents from flowing through the electronic circuit. The current flow through the electronic circuit 20 with the ESD protective arrangement 40 implemented in accordance with the present teachings is depicted in Fig. 3(c).

Fig. 4 is a first alternative embodiment of an illustrative implementation of the ESD protection arrangement constructed in accordance with the present teachings. In

Fig. 4, a third transistor M3 is provided in the path between the electronic circuit 20 and the source of voltage supply V_{dd}. The transistor M3 may be of similar design and construction as M2 but with a P-type channel. The third transistor M3 is biased by a third RC network including a third resistor R_3 and a third capacitor C_3. As the second transistor M2 is biased to allow current to flow therethrough in a normal (non-ESD) mode of operation, the third transistor M3 is biased to allow current to flow in a normal mode of operation and to inhibit current flow during an ESD event.

Those skilled in the art will appreciate that the switch may be located in the ground path, the supply path or both (as depicted in Fig. 4) within the scope of the present teachings.

Fig. 5 is a second alternative embodiment of an illustrative implementation of the ESD protection arrangement constructed in accordance with the present teachings. Fig. 5 depicts yet another alternative in which the switch M2 is depicted in line with the input terminal to the electronic circuit 20 being protected. The embodiment of Fig. 5 is similar to that of Fig. 3 with the most notable exception being the connection of the switch M2 in the input path of the electronic circuit.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof. For example, the invention is not limited to the location of the switch nor the implementation thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

I CLAIM:

CLAIMS

1. An arrangement for protecting an element from electro-static discharge comprising:

first means connected to an input terminal of said element for shunting a pulse of energy associated with an electro-static discharge having a time constant around said element and

second means connected to an input terminal of said element for for inhibiting the flow of said energy through said element.

2. The invention of Claim 1 wherein said second means is a switch having first, second and third terminals, said first terminal being a control terminal.

3. The invention of Claim 2 wherein the second and third terminals of said switch are connected to said element and ground respectively.

4. The invention of Claim 2 wherein the second and third terminals of said switch are connected to said element and a source of supply voltage respectively.

5. The invention of Claim 2 wherein the second and third terminals of said switch are connected to said element and an input terminal thereto respectively.

6. The invention of Claim 2 wherein said switch is a transistor switch.

7. The invention of Claim 6 wherein said transistor switch is an enhancement mode n-channel metal-oxide semiconductor transistor.

8. The invention of Claim 7 including a resistor connected between an input terminal of said transistor and the positive supply.

9. The invention of Claim 8 further including a capacitor connected between said input terminal of said transistor and ground.

10. The invention of Claim 9 wherein a time constant of said resistor and said capacitor is larger than the time constant of the electro-static discharge.

11. The invention of Claim 10 wherein the time constant of said resistor and said capacitor is larger than the time constant of the electro-static discharge by an order of magnitude.

12. An arrangement for protecting an element from electro-static discharge comprising:

a transistor switch responsive to said first means for inhibiting the flow of said energy through said element;

a resistor connected between an input terminal of said transistor and the positive supply; and

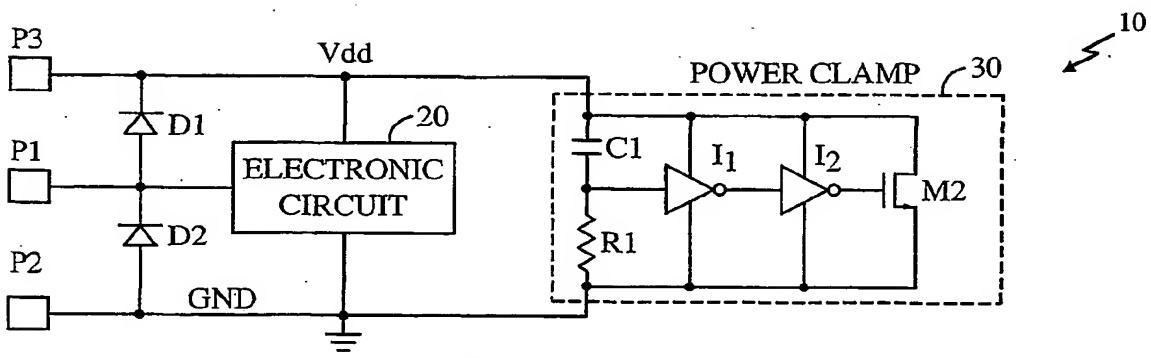
a capacitor connected between said input terminal of said transistor and ground.

13. The invention of Claim 14 wherein said transistor switch is an enhancement mode n-channel metal-oxide semiconductor transistor.

14. An method for protecting an element from electro-static discharge including the steps of:

sensing a pulse of energy associated with an electro-static discharge and providing a control signal in response thereto and

inhibiting the flow of said energy through said element in response to said control signal.



PRIOR ART

FIG. 1

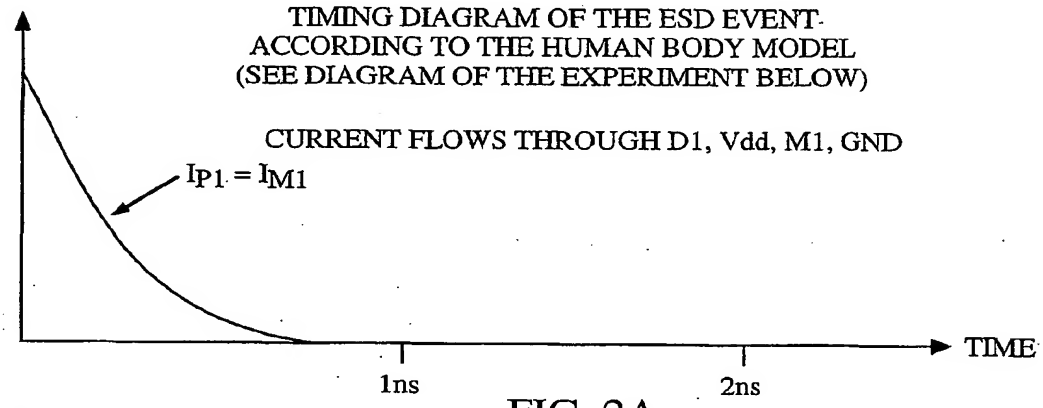


FIG. 2A

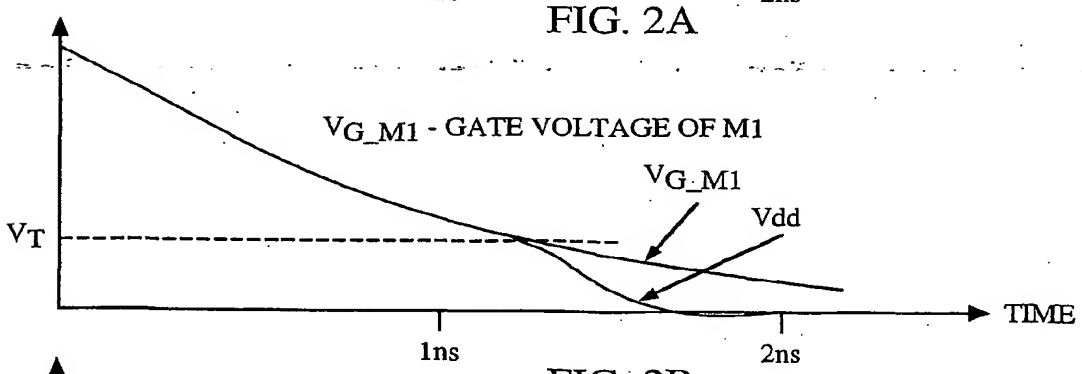


FIG. 2B

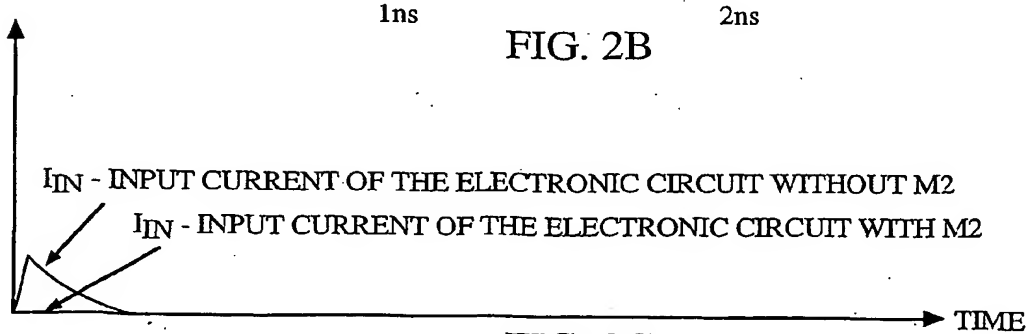


FIG. 2C

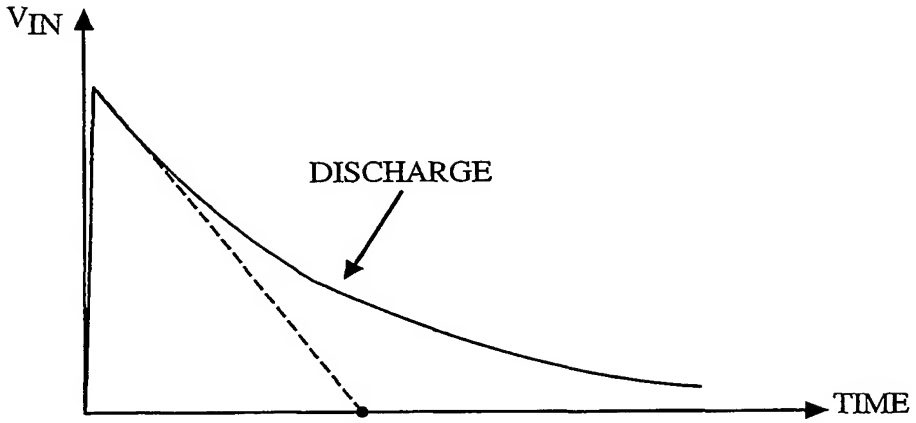

V_{IN}
DISCHARGE
TIME
T_{ESD} = 100pF - 1.5 KΩ
(DECAY TIME)

FIG. 2D

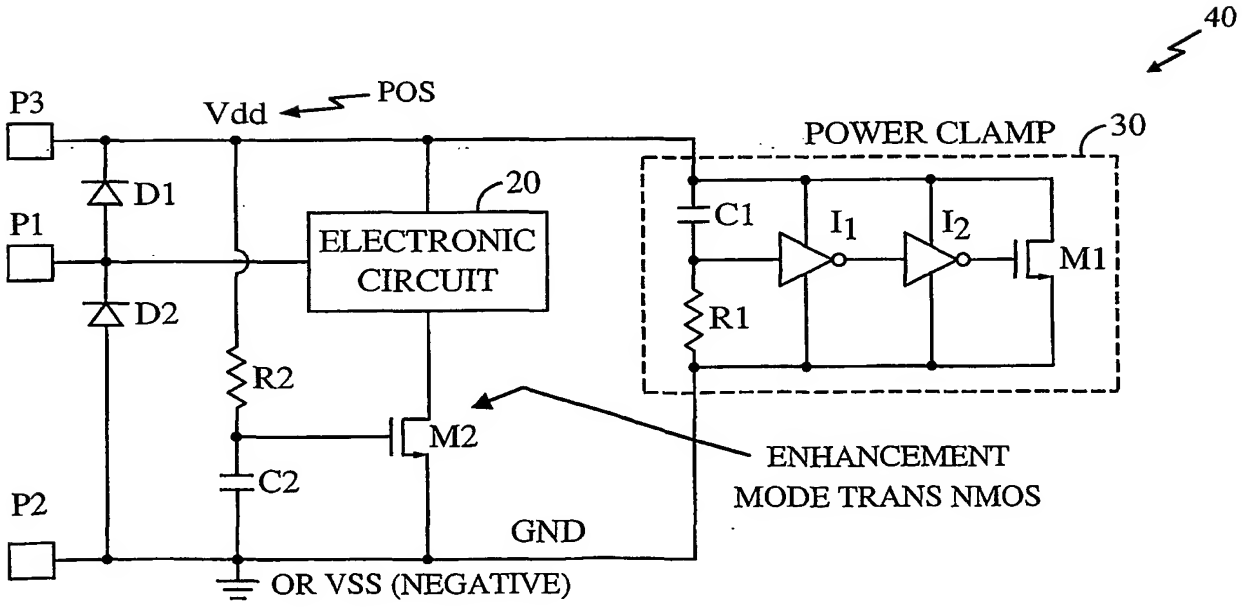

40
P3
Vdd
POS
POWER CLAMP
30
D1
20
P1
ELECTRONIC CIRCUIT
C1
I_1
I_2
M1
D2
R1
R2
M2
ENHANCEMENT MODE TRANS NMOS
C2
P2
GND
OR VSS (NEGATIVE)

FIG. 3

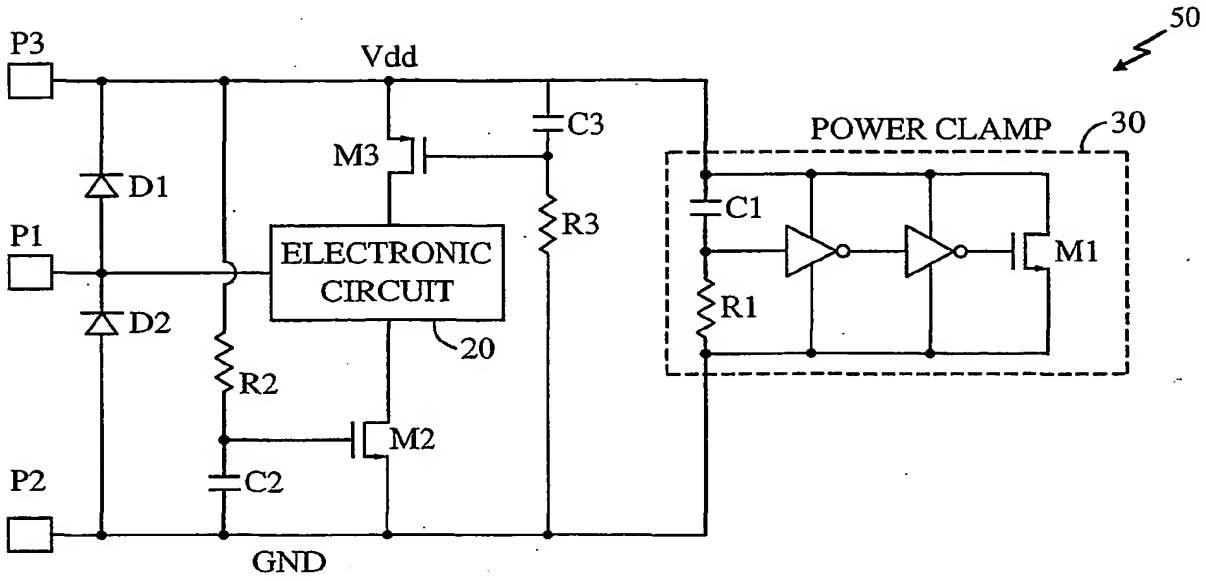

50
P3
Vdd
C3
POWER CLAMP
30
M3
D1
C1
P1
ELECTRONIC CIRCUIT
R3
M1
D2
20
R1
R2
M2
P2
C2
GND

FIG. 4

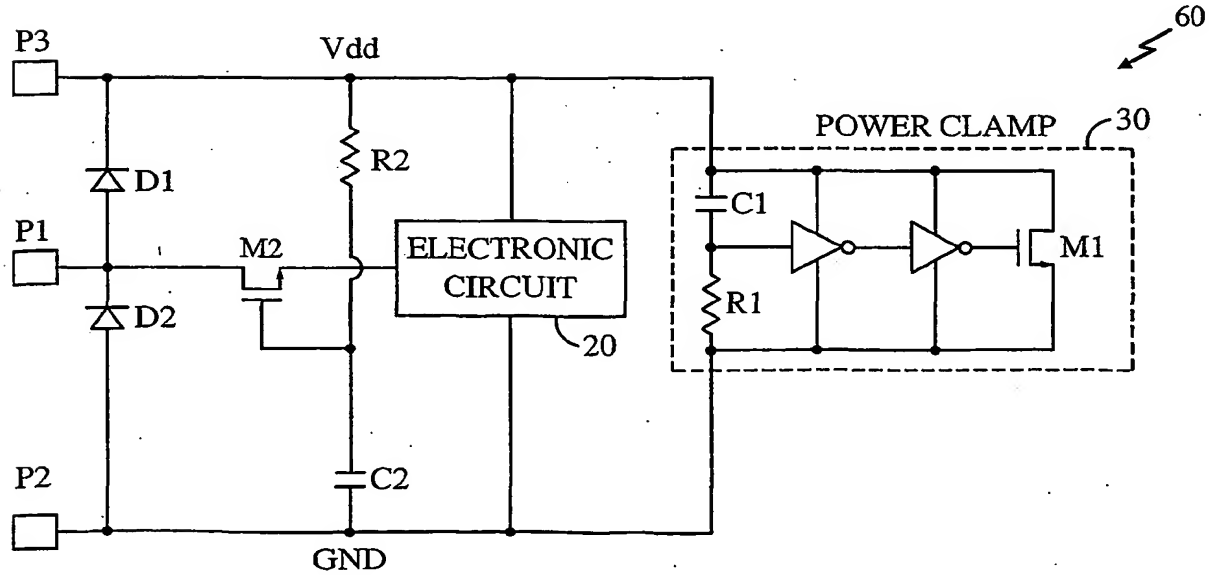

60
P3
Vdd
POWER CLAMP
30
R2
D1
C1
P1
M2
ELECTRONIC CIRCUIT
M1
D2
20
R1
P2
C2
GND

FIG. 5